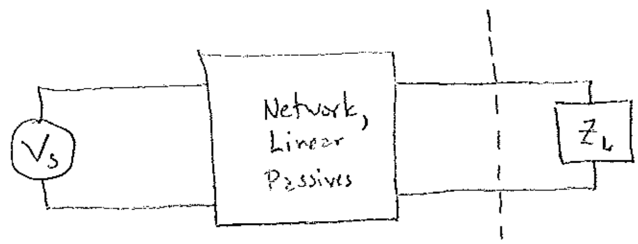
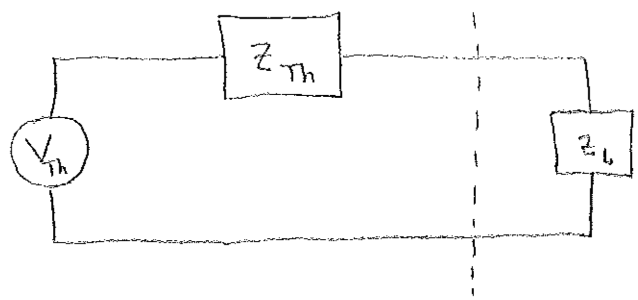
# Thevenin's Theorem

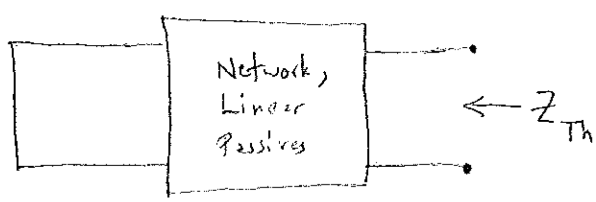
Consider a network of linear, passive components feed with a voltage source $V_s$ and a load attached to it :



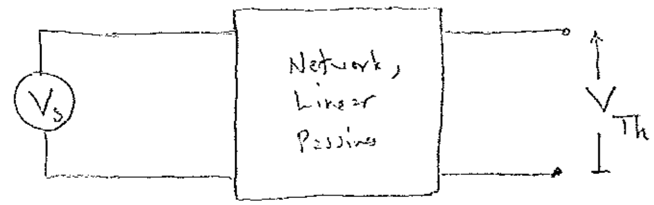

Then the circuit to the left of the dashed line is equivalent, as far as the load is concerned, to the circuit




where the Thevenin impedance $Z_{Th}$ is the impedance seen looking left from the dashed line when the voltage source $V_s$ is shorted :

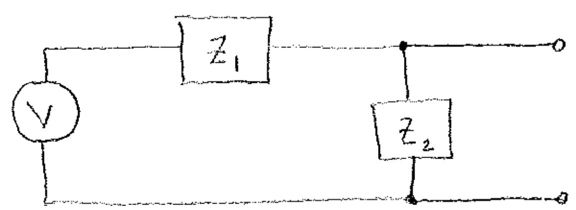



and the Thevenin voltage source $V_{Th}$ is the open circuit voltage at the dashed line when the load is removed :




The Thevenin equivalent circuit is a good way to simplify some complicated circuits, as it can be easier to apply than Kirchoff's network equations. It is used together with the:

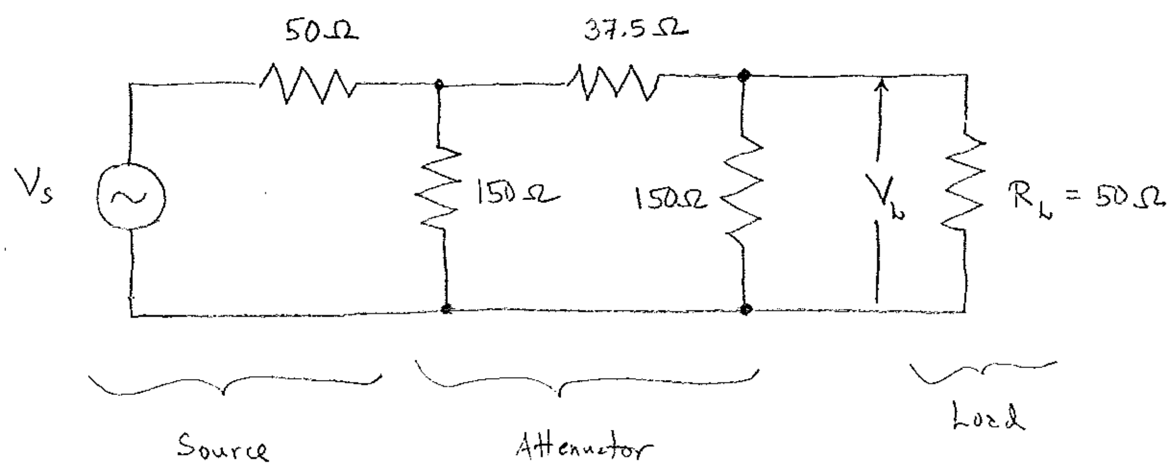
## Voltage Divider Rule



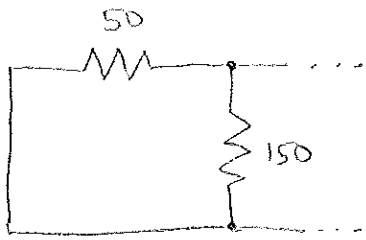

$$V_{out} = \frac{Z_2}{Z_1 + Z_2} V$$

## Example

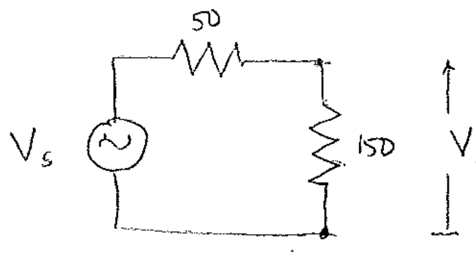
Find the voltage at the load of the following circuit:



We will apply Thevenin's Theorem twice. First we treat the two resistors on the left as the network:



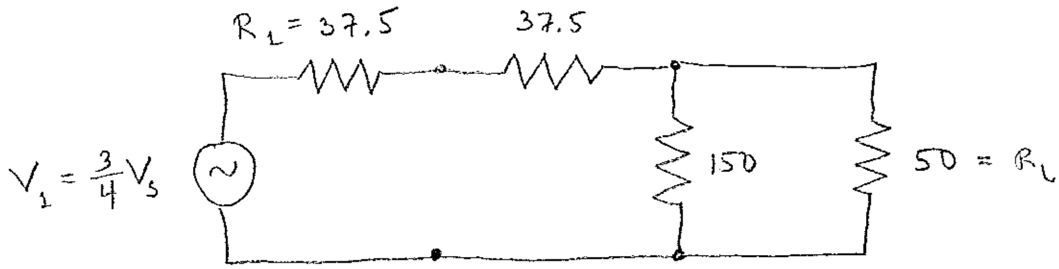

$$\leftarrow R_1 = 50 \parallel 150 = \frac{1}{\frac{1}{50} + \frac{1}{150}} = 37.5$$



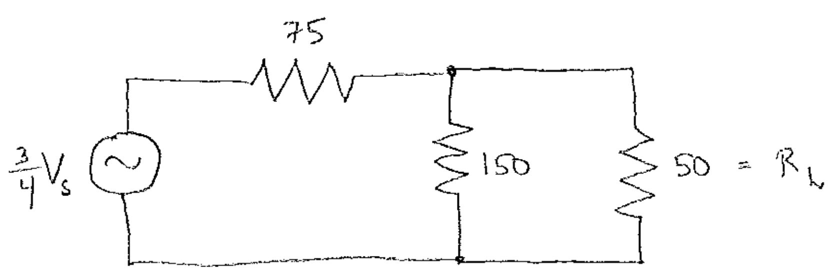

$$V_1 = V_s \frac{150}{50 + 150} = \frac{3}{4} V_s$$

(Voltage divider rule)

We get the equivalent circuit

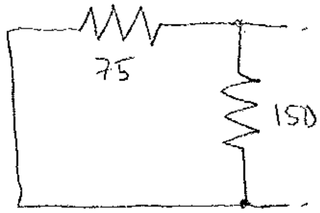



Combining the two $37.5\,\Omega$ resistors in series, we get

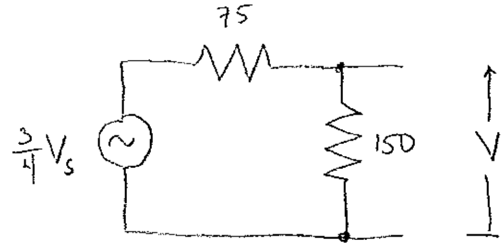



At this point we could simply combine the $150\,\Omega$ and $R_L = 50\,\Omega$ resistors and use the voltage divider rule, but let's use Thevenin again for illustrative purposes.

Treating the 75 Ω and 150 Ω resistors as the network we get



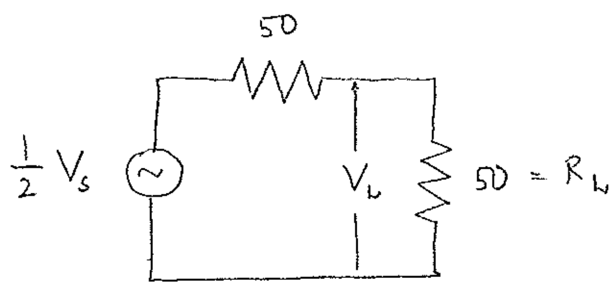
$$\leftarrow R_2 = 75 \parallel 150 = \frac{1}{\frac{1}{75} + \frac{1}{150}} = 50\,\Omega$$



$$V_2 = \left(\tfrac{3}{4} V_s\right) \frac{150}{75 + 150} = \left(\tfrac{3}{4} V_s\right) \tfrac{2}{3}$$

$$= \tfrac{1}{2} V_s$$

The final equivalent circuit is



and by the voltage divider rule

$$V_L = \frac{50}{50 + 50} \cdot \tfrac{1}{2} V_s = \tfrac{1}{2} \cdot \tfrac{1}{2} V_s = \tfrac{1}{4} V_s$$

We see that the attenuator circuit between a 50 Ω source and a 50 Ω load reduces the voltage by 1/4-th which is a

$$20 \log_{10}\left(\frac{V_L}{V_s}\right) = 20 \log_{10}\left(\frac{\tfrac{1}{4} V_s}{V_s}\right)$$

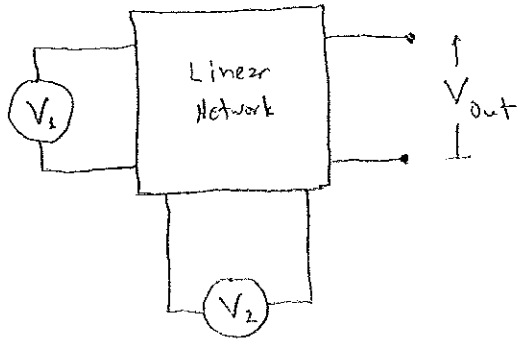
$$= 20 \log_{10}\left(\tfrac{1}{4}\right) = -12\text{ dB}$$

power reduction.

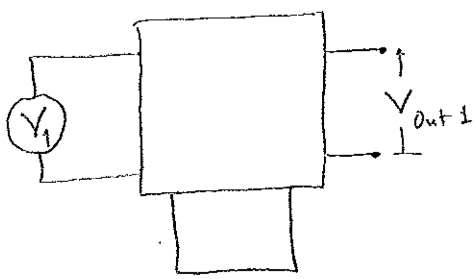
There is one additional rule applied when there is more than one voltage source:

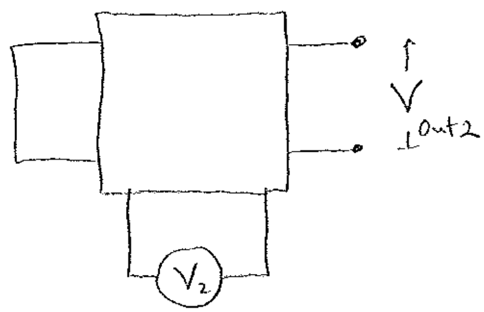
## The Superposition Rule

Suppose we have a linear network with two <u>independent</u> voltage sources:




Then $V_{out} = V_{out\,1} + V_{out\,2}$ where



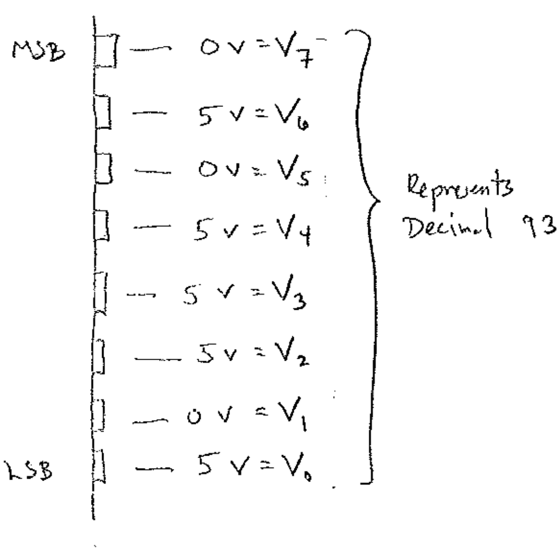

This generalizes in the obvious way to more than two independent sources.

# The R/2R Digital-to-Analog Converter

Suppose we want to convert a binary number at a microcontroller port to an analog voltage between zero and the system "logical 1" voltage $V_s$. Each pin of the port is either at 0 volts for a binary zero or $V_s$ volts for a binary one.

Label the pin voltages as $V_0, V_1, \ldots, V_{n-1}$ where $V_0$ corresponds to the least significant bit (1's bit) and $V_{n-1}$ is for the most significant bit.

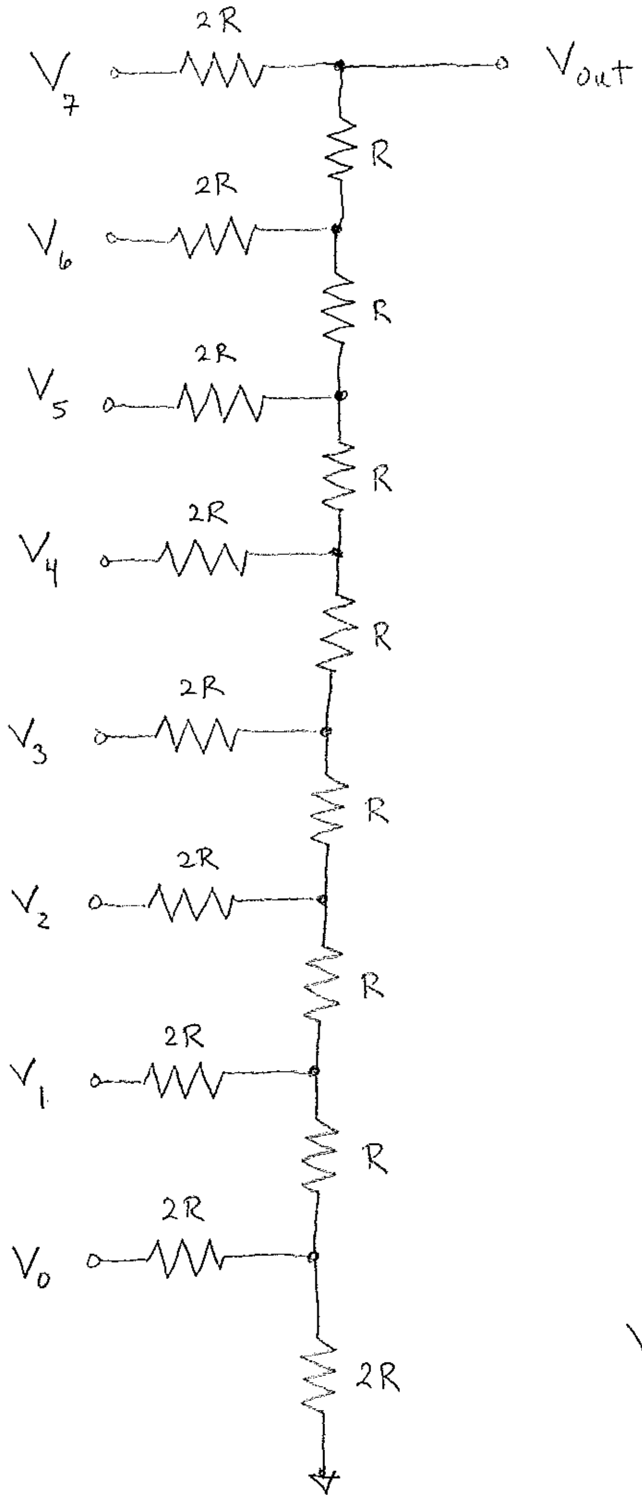
Example: An 8-bit port contains the binary value 01011101, which is a decimal 93. The least sig. bit is 1, the most sig. bit is 0. On a +5 v system the eight port pins have voltages 0 or $5 = V_s$:




The largest number on this port is 11111111 which is 255 and the smallest is 0 so we want an analog voltage of

$$\frac{93}{256} \cdot V_s = \frac{93}{256} \cdot 5 \cong 1.8164 \text{ v}$$

The following circuit is an 8-bit R/2R DAC




The R value can be anything reasonable, but preferably all resistors are 1% and matched.

Use two 2R resistors in parallel to get R, thus we need 23 resistors of value 2R

This circuit's output should be connected to a high impedance circuit like an op amp to avoid pulling down $V_{out}$.

$$V_{out} = \sum_{m=0}^{8} \frac{D_m}{2^{8-m}} V_s$$

$$= \left( \frac{D_0}{2^8} + \frac{D_1}{2^7} + \cdots + \frac{D_7}{2} \right) V_s$$

where $D_m$ is binary value of the m-th bit,

$$V_m = \begin{cases} 0 & \text{if } D_m = 0 \\ V_s & \text{if } D_m = 1 \end{cases}$$

For our example 01011101 we have

$$V_{out} = \left(\frac{1}{256} + \frac{0}{128} + \frac{1}{64} + \frac{1}{32} + \frac{1}{16} + \frac{0}{8} + \frac{1}{4} + \frac{0}{2}\right) V_s$$

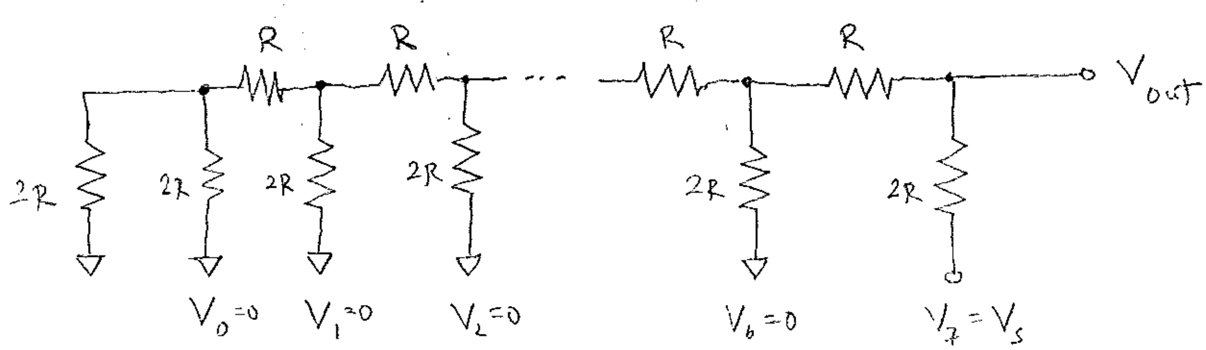
$$= \frac{1 + 0 + 4 + 8 + 16 + 0 + 64 + 0}{256} \quad V_s$$

$$= \frac{93}{256} \cdot V_s = \frac{93}{256} \cdot 5 \cong 1.8164 \text{ v}$$

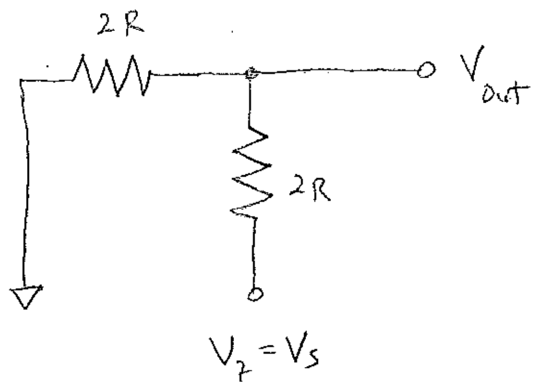
as we desired. The analog outputs are 256 discrete values between 0 and $\frac{255}{256} = 0.99609375$ times $V_s$, not quite $V_s$, but close.

We can use Thevenin's Theorem, the voltage divider rule, and the superposition rule to verify the equation for the output voltage. By the superposition rule we only need to prove the equation for binary values with only one 1 bit, that is, only one of the port pin voltages $V_m$ is $V_s$ and the others are 0 (at ground).

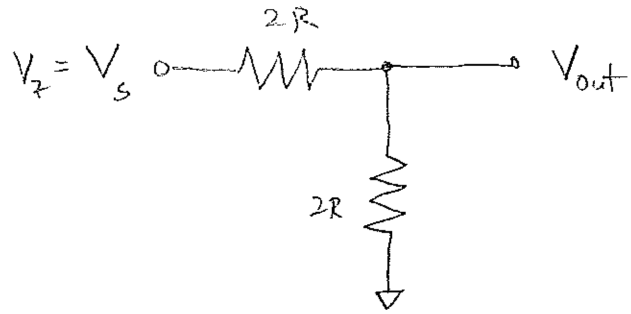
Consider $V_7 = V_s$, $V_6 = \cdots = V_0 = 0$.



starting at the left end we combine the resistors using the parallel and series equivalents. The equivalent circuit is just




or

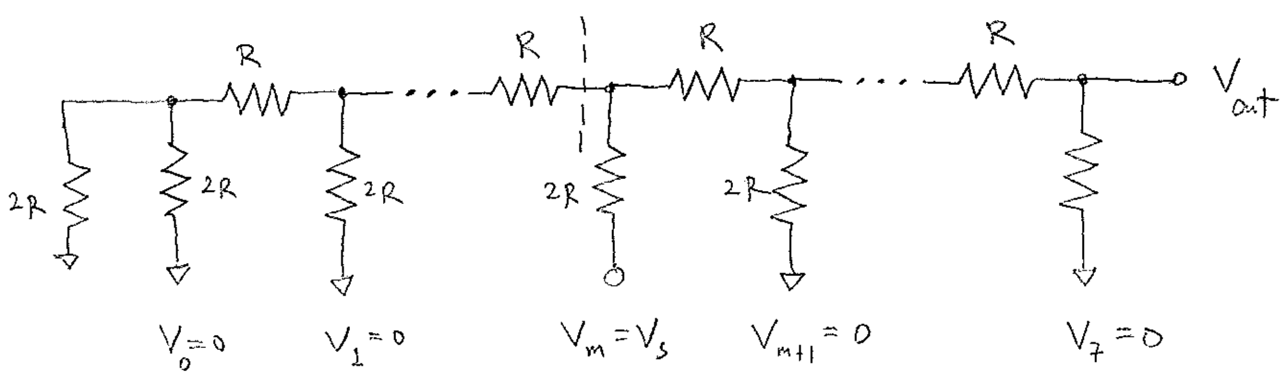



and the voltage divider rule gives

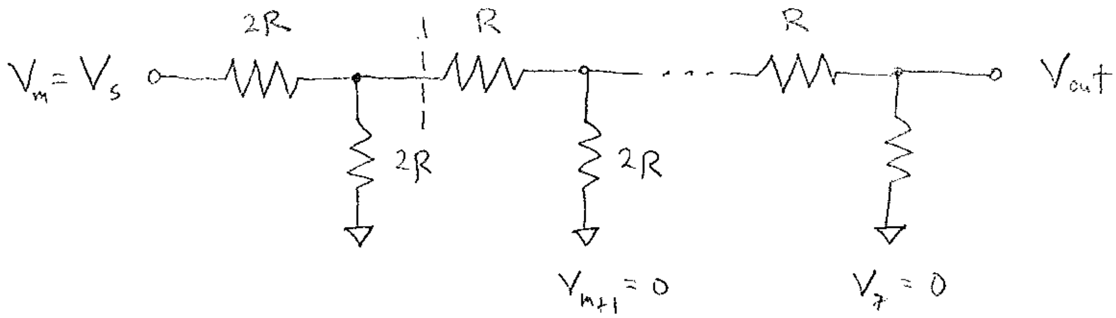
$$V_{out} = \frac{2R}{2R + 2R} V_s = \frac{1}{2} V_s$$

$$= \left( \frac{0}{2^8} + \frac{0}{2^7} + \cdots + \frac{0}{2^2} + \frac{1}{2^1} \right) V_s$$

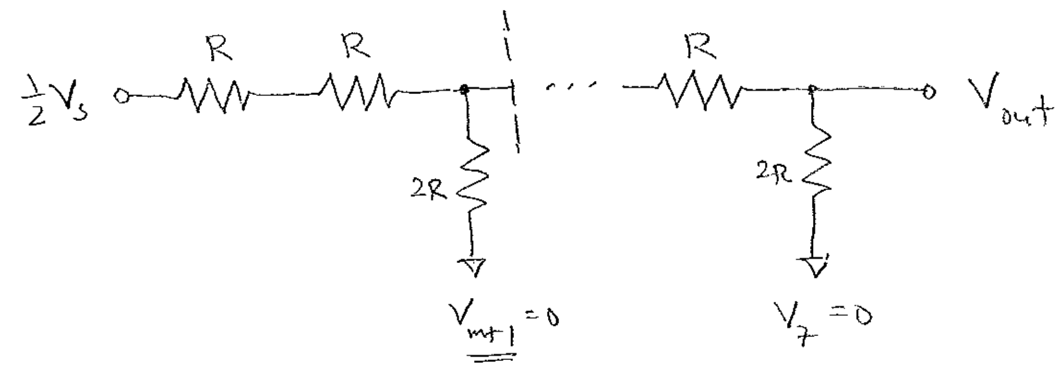
and the formula for $V_{out}$ is verified for one case. For the remaining 7 cases, let $V_m = V_s$ for some $m$ between 0 and 6 and set all other input voltages to zero. The circuit is

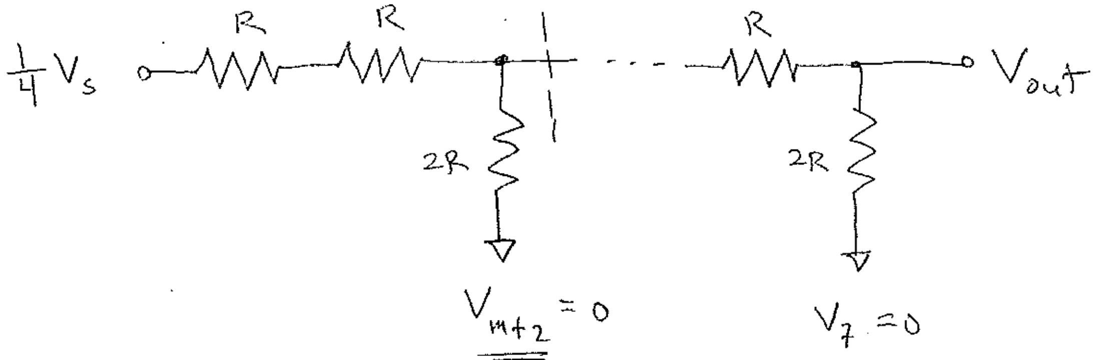


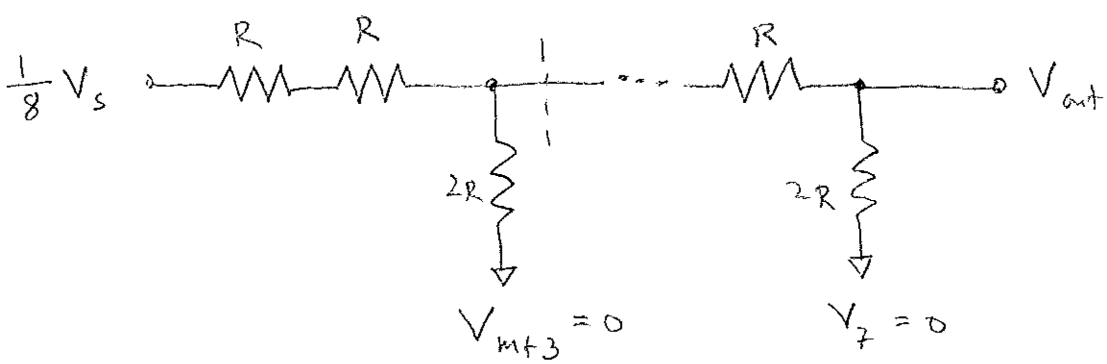
Combine the resistors to the left of the dashed line to get




We now apply Thevenin several times to get equivalent circuits :

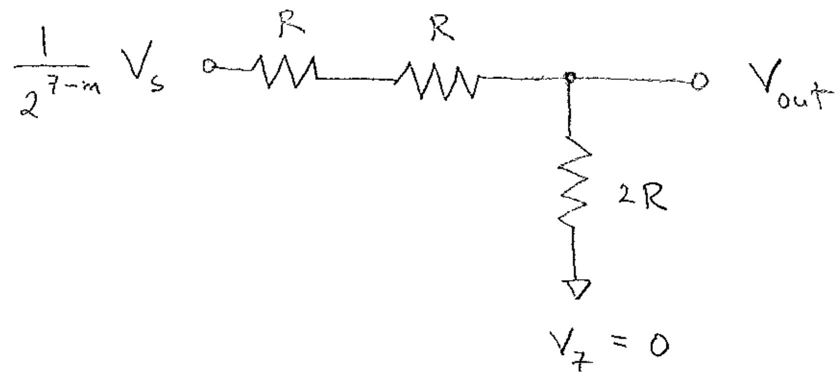



Etc.

We end up with




and by the voltage divider rule

$$V_{out} = \frac{1}{2}\left(\frac{1}{2^{7-m}} V_s\right) = \frac{1}{2^{8-m}} V_s$$

This is the desired result. Combining by superposition all the cases,

$$V_{out} = \left(\frac{D_0}{2^8} + \frac{D_1}{2^7} + \cdots + \frac{D_6}{2^2} + \frac{D_7}{2}\right) V_s$$